ESE Multimeter

Design

Requirements

* 0-.1V
* 0-1V
* 0-10V
* 0-.001A
* 0-.01A
* 0-.1A
* 10-10kOhm
* Be built with as many on hand parts as possible
* Minimum cost (for what is in stock)

Decisions

* Shunt resistors chosen to provide low burden voltage and coincide with the lowest voltage sense range
* Shunt resistors are only 1% to reduce cost since the panel meter is of limited precision
* Opamp chosen as it was on hand and provides near rail-rail performance
* Vdd and Vss chosen to allow for full 0-10v input
* All passives were selected for what was available on hand

**Overview**

The signal enters through the binding post. From there is passes through the polarity and over-voltage protection circuit. Polarity is enforced by a pmos with its gate connected to ground. Overvoltage protection is provided a Zener clamped pmos driving the gate of another pmos in-line with the input. An led alerts the operator that the input has exceeded allowable limits.

At the output of the protection circuit are the three sensing circuits. The resistance sense circuit is a Wilson current source constructed from 4 3904 PNP bipolar junction transistors. This source delivers 1mA into the input terminal. For current sensing a series of three shunt resistors is used. These are tapped off using p-channel mosfets and present a voltage to the opamp. This opamp provides the ultimate sensing for all modes. The opamp is a TLV274 in a non-inverting configuration. Voltage and resistance ranges are accounted for by selecting the gain. For the 0-10V range a unity gain is used. Circuit gain is selected through pmos and defaults to an A of 100. The output of the opamp passes through a current limiting resistor and then through the meter movement. The voltage across the meter is clamped to 10V with a Zener diode and a led to provide out of range indication.

At the appropriate current ranges the max burden voltage should be 100mV.

Power for the meter is derived from a 9v battery. A Dickson charge pump is used to step up Vbat to ~18V which is then regulated down to 12V with an LDO. The negative voltage rail uses a voltage inverter and an LDO to create the 1.2V offset voltage. Timing for switching the diver mosfets is provided by a 555. The device is configured to run in astable mode at a frequency near its 500kHz limit. This is done to limit the losses in the charge pump.

The gates of the PMOS are pulled high to Vdd which is greater than the maximum allowed input so as to force the mosfets off in all input conditions. Similarly, the mosfet gates are pulled low to Vss when in use. Vss was selected to be greater than Vth so that the mosfet will remain on when the input is ~0V.